WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

at least one external node;

operational circuitry configured to operate in response to at least one control signal; and

test circuitry coupled to the external node and the operational circuitry, wherein the test circuitry is configured to operate in at least one test mode in response to test data received at the external node from an external source, and the test circuitry is configured to assert to the operational circuitry a control signal in response to an external control signal received at the external node.

2. The integrated circuit of claim 1, wherein the test circuitry is configured to extract the test data from an amplitude-modulated input signal asserted to the external node from the external source, and to generate the control signal in response to the input signal.

3. The integrated circuit of claim 2, wherein the external control signal is a binary signal determined by the input signal, and the test circuitry is operable in a mode in which the control signal is a binary signal whose state is determined by the state of the external control signal.

4. The integrated circuit of claim 2, wherein the test circuitry is configured to extract a clock signal from the input signal, and to operate in response to the clock signal during said at least one test mode.

5. The integrated circuit of claim 2, wherein the input signal has at least three levels, including a low level below a first threshold, a high level above a second threshold, and an intermediate level between the first threshold and the

second threshold, and wherein the test circuitry includes:

first comparator circuitry, coupled to receive the input signal and configured to operate in a first mode in which said first comparator circuitry generates a first signal indicative of whether the input signal has a level less than the first threshold; and

second comparator circuitry, coupled to receive the input signal and configured to operate in a first mode in which said second comparator circuitry generates a second signal indicative of whether the input signal has a level greater than the second threshold.

6. The integrated circuit of claim 5, wherein the test circuitry also includes:

a flip-flop having a set terminal, a reset terminal, and an output, wherein the set terminal is coupled to receive the second signal, the reset terminal is coupled to receive the first signal, the output asserts a data signal in response to the first signal and the second signal, and the data signal is indicative of the test data.

7. The integrated circuit of claim 5, wherein the test circuitry includes logic circuitry coupled and configured to generate a second control signal in response to the input signal, and to assert the second control signal to the first comparator circuitry and the second comparator circuitry, wherein the second control signal is indicative of whether the input signal has a level that has remained below the first threshold for at least a predetermined minimum time, and wherein the second control signal disables each of the first comparator circuitry and the second comparator circuitry from operating in the first mode when the second control signal indicates that the level of input signal has remained below the first threshold for at least the predetermined minimum time.

8. The integrated circuit of claim 5, wherein the input signal has at least four levels, including a latch level above a third threshold, where the third threshold is greater than the second threshold, and wherein the test circuitry includes:

third comparator circuitry, coupled and configured to generate a latch signal indicative of whether the input signal has a level greater than the third threshold.

9. The integrated circuit of claim 2, wherein the test circuitry includes:

comparator circuitry coupled and configured to receive the input signal, to extract the test data from the input signal, and to extract a latch signal from the input signal, wherein the latch signal is indicative of whether the input signal has a level exceeding a latch threshold; and

at least one register coupled to the comparator circuitry for receiving the latch signal and at least some of the test data.

10. The integrated circuit of claim 9, wherein the test circuitry includes:

a nonvolatile memory comprising at least one programmable cell having a first input coupled to receive a sequence of bits of the test data, and a second input coupled to receive a programming voltage, wherein the cell is operable in a mode in which the cell stores one of the bits of the test data being asserted at the first input while the programming voltage exceeds a programming level.

11. The integrated circuit of claim 10, also including:

a switch, coupled between the external node and the second input of the cell, wherein the switch has a closed state in which it passes the input signal to the second input of the cell, and wherein the input signal is said programming voltage.

12. The integrated circuit of claim 11, wherein the input signal includes a programming pulse having a leading edge, and a level that rises to at least the latch threshold at the leading edge, and then reaches the programming level without falling below the latch threshold, and then falls to below the latch threshold, whereby said one of the bits of the test data at the first input of the cell is stored in said cell in response to the programming pulse of the input signal.

13. The integrated circuit of claim 2, wherein the test circuitry includes:

a nonvolatile memory comprising at least one programmable cell having a first input coupled to receive a sequence of bits of the test data, and a second input coupled to receive a programming voltage, wherein the cell is operable in a mode in which the cell stores one of the bits of the test data being asserted at the first input while the programming voltage exceeds a programming level.

14. The integrated circuit of claim 1, wherein the at least one test mode includes a first test mode, and the test circuitry is configured to assert data to the external node, for transmission to external circuitry, during the first test mode.

15. The integrated circuit of claim 14, wherein the first test mode is a measurement mode, and the test circuitry is configured to assert measurement data to the external node during the measurement mode.

16. The integrated circuit of claim 1, wherein the test circuitry is configured to extract the test data from an input signal asserted to the external node from the external source, and wherein the test circuitry includes:

a timeout circuit coupled and configured to terminate operation of the test circuitry in each said test mode unless bits of the test data occur at the external node with frequency not less than a predetermined minimum frequency.

17. The integrated circuit of claim 1, wherein the test circuitry includes:

logic circuitry coupled and configured to extract the test data from an input signal asserted to the external node from the external source;

lock circuitry coupled to receive the test data, and operable to analyze the test data to determine whether said test data is indicative of a digital key, and to generate a second control signal in response to determining that said test data is indicative of the digital key; and

additional circuitry, coupled to the logic circuitry and configured to perform at least one test mode operation when the test circuitry is in each said test mode, wherein the lock circuitry asserts the second control signal to the additional circuitry to initiate each said test mode of the test circuitry.

18. The integrated circuit of claim 17, wherein the lock circuitry is a state machine operable in each of at least a begin state, a decision state, a test-mode enable state, and an error state, wherein the state machine in the begin state is ready to analyze a bit of the test data to determine whether said bit is an element of the digital key, the state machine in the decision state has received at least one bit of the test data but has not determined whether the test data is indicative of the digital key, the state machine in the test-mode enable state has received at least one bit of the test data and determined that the test data received thereby is indicative of the digital key, and the state machine in the error state has received at least one bit of the test data and determined that the test data received thereby is not indicative of the digital key.

19. The integrated circuit of claim 18, wherein the state machine is configured to remain in the decision state for no more than a predetermined interval of time commencing on entry into the decision state, and to undergo a transition from the decision state to the error state if said state machine has not

undergone a transition from the decision state to one of the test-mode enable state and the error state during said predetermined interval of time commencing on entry into the decision state.

20. The integrated circuit of claim 18, wherein the state machine is configured to remain in the error state for at least a predetermined rest interval commencing on entry into said error state, and to undergo a transition from the error state to the begin state in response to first occurrence of a predetermined data structure of the input signal after said predetermined rest interval.

21. Test circuitry suitable for use in a circuit comprising an access node, and operational circuitry configured to operate in response to at least one control signal asserted to the access node, said test circuitry comprising:

logic circuitry configured to be coupled to the access node and to the operational circuitry; and

additional circuitry coupled to the logic circuitry and configured to operate in at least one test mode in response to test data received at the access node,

wherein the logic circuitry is configured to extract the test data from an amplitude-modulated input signal asserted to the access node when the logic circuitry is coupled to the access node, and to generate the control signal in response to the input signal and assert said control signal to the operational circuitry when the logic circuitry is coupled to the access node and to the operational circuitry.

22. The test circuitry of claim 21, wherein the logic circuitry is configured to extract a clock signal from the input signal, and to assert the clock signal to the additional circuitry, when the logic circuitry is coupled to the access node and to the operational circuitry, and the additional circuitry is

configured to operate in response to the clock signal during said at least one test mode.

23. The test circuitry of claim 21, wherein the input signal has at least three levels, including a low level below a first threshold, a high level above a second threshold, and an intermediate level between the first threshold and the second threshold, and wherein the logic circuitry includes:

first comparator circuitry, configured to be coupled to receive the input signal and to operate in a first mode in which said first comparator circuitry generates a first signal indicative of whether the input signal has a level less than the first threshold; and

second comparator circuitry, configured to be coupled to receive the input signal and to operate in a first mode in which said second comparator circuitry generates a second signal indicative of whether the input signal has a level greater than the second threshold.

24. The test circuitry of claim 23, wherein the logic circuitry also includes:

a flip-flop having a set terminal, a reset terminal, and an output, wherein the reset terminal is coupled to receive the first signal, the set terminal is coupled to receive the second signal, the output asserts a data signal in response to the first signal and the second signal, and the data signal is indicative of the test data.

25. The test circuitry of claim 23, wherein the input signal has at least four levels, including a latch level above a third threshold, where the third threshold is greater than the second threshold, and wherein the logic circuitry includes:

third comparator circuitry, coupled and configured to generate a latch

signal indicative of whether the input signal has a level greater than the third threshold.

26. The test circuitry of claim 21, wherein the additional circuitry includes:

a nonvolatile memory comprising at least one programmable cell having a first input coupled to receive a sequence of bits of the test data, and a second input coupled to receive a programming voltage, wherein the cell is operable in a mode in which the cell stores one of the bits of the test data being asserted at the first input while the programming voltage exceeds a programming level.

27. The test circuitry of claim 21, wherein the logic circuitry includes:

comparator circuitry coupled and configured to receive the input signal, to extract the test data from the input signal, and to extract a latch signal from the input signal, wherein the latch signal is indicative of whether the input signal has a level exceeding a latch threshold, and

wherein the additional circuitry includes:

at least one register coupled to the comparator circuitry for receiving the latch signal and at least some of the test data;

a nonvolatile memory comprising at least one programmable cell having a first input coupled to receive a sequence of bits of the test data, and a second input coupled to receive a programming voltage, wherein the cell is operable in a mode in which the cell stores one of the bits of the test data being asserted at the first input while the programming voltage exceeds a programming level; and

a switch, coupled between the access node and the second input of the cell, wherein the switch has a closed state in which it passes the input signal to the second input of the cell, and wherein the input signal is said programming voltage.

28. A method for controlling, and performing at least one of testing, configuration, and reconfiguration, of operational circuitry within an integrated circuitry, wherein the integrated circuitry has an external node and the operational circuitry is configured to operate in response to at least one control signal, said method including the steps of:

operating test circuitry of the integrated circuit in at least one test mode in response to test data received at the external node from an external source; and

asserting said at least one control signal from the test circuitry to the operational circuitry in response to an external control signal received at the external node.

29. The method of claim 28, including the step of:

extracting the test data from an amplitude-modulated input signal asserted to the external node from the external source, and generating said at least one control signal in response to the input signal.

30. The method of claim 29, also including the step of:

extracting a clock signal from the input signal.

31. The method of claim 30, also including the step of:

operating the test circuitry in response to the clock signal during said at least one test mode.

32. The method of claim 29, wherein the input signal has at least three levels, including a low level below a first threshold, a high level above a second threshold, and an intermediate level between the first threshold and the second threshold, and the step of extracting the test data from the input signal includes the steps of:

generating a first signal indicative of whether the input signal has a level less than the first threshold;

generating a second signal indicative of whether the input signal has a level greater than the second threshold; and

asserting the first signal to a reset terminal of a flip-flop and asserting the second signal to a set terminal of the flip-flop, thereby causing the flip-flop to assert a data signal indicative of the test data.

33. The method of claim 29, wherein the test circuitry includes a nonvolatile memory comprising at least one programmable cell, and said method also includes the steps of:

during each said test mode, generating a latch signal in response to determining that the input signal has a level above a latch threshold; and

capturing a bit of the test data at said cell in response to the latch signal.

34. The method of claim 33, also including the step of:

after capturing the bit of the test data at said cell, asserting a voltage having a programming level to the cell, wherein the programming level is above the latch threshold, thereby storing said bit of the test data in the cell.

35. The method of claim 28, also including the step of:

during said at least one test mode, operating the test circuitry to assert data to the external node for transmission to external circuitry.

36. The method of claim 28, also including the steps of:

extracting the test data from an amplitude-modulated input signal asserted to the external node from the external source; and

when operating the test circuitry in each said test mode, terminating test mode operation of the test circuitry unless bits of the test data occur at the

external node with frequency not less than a predetermined minimum frequency

37. The method of claim 36, also including the step of:
generating said at least one control signal in response to the input signal.

38. The method of claim 28, also including the steps of:

extracting the test data from an input signal asserted to the external node from the external source; and

analyzing the test data to determine whether said test data is indicative of a key, and commencing operation of the test circuitry in each said test mode only in response to determining that said test data is indicative of the key.

39. The method of claim 38, wherein the step of analyzing the test data to determine whether said test data is indicative of the key is performed by placing a state machine in a begin state in which the state machine is ready to analyze a bit of the test data to determine whether said bit is an element of the key, then operating the state machine in a decision state in which the state machine has received at least one bit of the test data but has not determined whether the test data is indicative of the key, and placing the state machine in a test-mode enable state when the state machine has received at least one bit of the test data and determined that the test data received thereby is indicative of the key, wherein the method also includes the step of:

placing the state machine in an error state when the state machine has received at least one bit of the test data and determined that the test data received thereby is not indicative of the digital key.

40. The method of claim 39, wherein the method includes the step of:

operating the state machine in the decision state for no more than a predetermined interval of time commencing on entry into said decision state,

and causing the state machine to undergo a transition from the decision state to the error state if said state machine has not undergone a transition from the decision state to one of the test-mode enable state and the error state during said predetermined interval of time commencing on entry into the decision state.